



LOUIS POBLETE ALARCÓN

Analog Devices, Inc. (ADI) Professor for Microelectronics
Electrical and Electronics Engineering Institute (EEEI)
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Contact Information

Microelectronics and Microprocessors Laboratory (MICROLAB)
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Education

- 2010 UNIVERSITY OF CALIFORNIA, BERKLEY
Doctor of Philosophy in Electrical Engineering and Computer Science, December 2010
- 2002 UNIVERSITY OF THE PHILIPPINES
Master of Science in Electrical Engineering, October 2002
- 1995 UNIVERSITY OF THE PHILIPPINES
Bachelor of Science in Electrical Engineering (magna cum laude), April 1995

Academic Positions

- 2013– Analog Devices, Inc. (ADI) Professor of Microelectronics, EEEI University of the Philippines, Diliman
- 2010– Laboratory Head, Microelectronics and Microprocessors Laboratory (MICROLAB), EEEI University of the Philippines, Diliman
- 2004–2010 EECS Ph.D. Student, University of California, Berkeley
- 1998–2004 Assistant Chair, UP EEEI (formerly the EEE Department)
- 1995–2004 Laboratory Head, the Microelectronics and Microprocessors Laboratory (MICROLAB), EEEI University of the Philippines, Diliman
- 1995– Faculty Member, EEEI, University of the Philippines Diliman

Research Interests

Low voltage and low energy integrated circuits; Low energy computation; Integrated sensor nodes and networks for environmental monitoring; Integrated energy harvesting; Asynchronous circuits

Research Projects:

Center for Integrated Circuits and Devices (CIDR) - Program Leader
EEEI, UP Diliman 2022–present

Resilient Sensory Swarms for Energy and Environmental Monitoring (RESE2NSE) - Program Leader
EEEI, UP Diliman 2015–2021

The SmartWire Project - Program Leader
EEEI, UP Diliman 2011–2016

Low Energy Asynchronous Computation Using Sense Amplifier-based Pass Transistor Logic (SAPTL)
BWRC, UC Berkeley 2006-2010

Low Energy Active RFID Baseband Processor
BWRC, UC Berkeley 2009-2010

Professional Affiliations

Institute of Electrical and Electronics Engineer (IEEE); IEEE Solid-State Circuits Society (SSCS)

Founding Chairperson, IEEE Solid-State Circuits Society (SSCS) Republic of the Philippines Section

Select Publications

- Legaspi, P., Alarcón, L., “Input Power Range Extension Using Duty-Cycling and Granularity Reduction in a 5.8GHz RF Energy Harvester Dynamic Matching Circuit”, The IEEE Region 10 Symposium (TENSYMP) 2021, August 23-25, 2021, Jeju, Republic of Korea
- M. D. Alea and L. P. Alarcón, “Gate Current Cancellation Using a Replica PMOS and Digital Feedback for Temperature-coefficient Reduction on an Ultra-low Power Voltage Reference,” 2021 4th International Conference on Circuits, Systems and Simulation (ICCSS), 2021, pp. 83-88, 26-28 May 2021, Virtual conference
- Chua, A., Maestro, R.J., Jardin, J.C., Monisit, K., Nuestro, R., Fabay, K.B., Pelayo, B.R., Lofamia, W.V., Ortiz, J.R., Madamba, J.A., Alarcón, L., “Smart-Wire: A 0.5V 44uW 0C to 100C Power-line Energy Harvesting Sensor Node”, 2017 IEEE Custom Integrated Circuits Conference (CICC), 1-3 May 2017. Austin, Texas.
- Bacquiran, Alvionne; Hizon, John Richard; Alarcon, Louis; “PVT-Aware Digital Techniques for a Power Line Energy-Harvesting Sensor Node”, in IEEE ISCAS 2016, May 22-26, 2016, Montreal, Canada
- Chua, A.N.; Maestro, R.J.M.; Alba, M.E.V.; Lofamia, W.V.V.; Fabay, K.B.; Jardin, J.C.; Jocson, K.J.; Pelayo, B.R.; Madamba, J.A.R.; Hizon, J.R.E.; Alarcon, L.P., “Delay Variation Compensation through Error Correction using Razor,” 6th International Workshop on CMOS Variability (VARI 2015). 1-4 September 2015, Bahia, Brazil.
- A. S. Luna, J. E. Hizon, and L. P. Alarcon, “Timing Analysis and Optimization of Voltage Scaled CMOS Digital Circuits with Dual-Vth Devices“, APCCAS 2014 – IEEE Asia Pacific Conference on Circuits and Systems, Nov 17-20, 2014, Ishigaki Island, Japan
- P. Magpantay, I. Paprotny, R. Send, Q. Xu, C. Sherman, L. Alarcon, R. White, and P. Wright, “Energy Monitoring in Smart Buildings Using Wireless Sensor Networks“, SMART 2014: The Third International Conference on Smart Systems, Devices and Technologies, Jul 20-24, 2014, Paris, France
- Markovic, D., Wang, C. C., Alarcón, L. P., Liu, T.-T., Rabaey, J. M., “Ultralow-Power Design in Near-Threshold Region”, Proceedings of the IEEE, vol.98, no.2, pp.237–252, Feb. 2010 (*Journal Citation Reports (JCR) from Thomson Reuters Impact Factor: 6.81*)
- Liu, T.-T., Alarcón, L. P., Pierson, M. D., Rabaey, J. M., “Asynchronous Computing in Sense Amplifier-Based Pass Transistor Logic”, Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.17, no.7, pp.883–892, July 2009 (*Journal Citation Reports (JCR) from Thomson Reuters Impact Factor: 1.219*)